REMARKS

Claims 1-6, 8-13, and 15-20 are all the claims pending in the application. Claims 7, 14, and 21 are cancelled, above. Claims 1-6, 8-13, and 15-20 stand rejected on prior art grounds. Applicant respectfully traverses this rejection based on the following discussion.

I. The Prior Art Rejections

Claims 1-6, 8-13, and 15-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Aguilar et al. (U.S. Patent No. 6,199,137), hereinafter referred to as Aguilar in view of Kukic et al., (U.S. Publication No. 2004/0213241), hereinafter referred to as Kukic. Applicants respectfully traverse these rejections based on the following discussion.

Applicant respectfully traverses this rejection because the prior art of record does not disclose selectively engaging different numbers of serial data lanes to alter the speed of data passing through a core to perform a speed reduction to accommodate different operating speeds of the transmission media and the processor.

The Office Action admits that Aguilar does not disclose selectively engaging serial data lanes to alter the speed of data passing through the core. The Office Action refers to Kukic for teaching selecting different numbers of links between multiplexors. The Office Action concludes that it would have been obvious to selectively engage the serial data lanes to alter the speed of data passing through the core.

However, Kukic only states (paragraph 22) that the number of links is selected, synchronized, and trained to operate at an optimal rate and Kukic does not mention anything concerning engaging different numbers of serial data lanes to alter the speed of data passing through a core to perform a speed reduction to accommodate different operating speeds of the transmission media and the processor.

Kukic goes on to explain that the number of links that are selected depends on a number of variables including: the data rate that the customer requests; the physical characteristics of each of the links; the number of available links; and other criteria

(paragraph 22). Nothing within paragraph 22 of Kukic suggests that different numbers of serial data lanes should be engaged to alter the speed of data passing through a core to perform a speed reduction to accommodate different operating speeds of the transmission media and the processor much less a multiplexor arranged to do so. Indeed Kukic only explains some of the criteria for selecting the number of links and provides an optimal rate for each group of selected links that are selected.

Therefore, it is Applicant's position that prior art of record does not teach or suggest the claimed operation "whereby said selector selectively engages different numbers of said serial data lanes to alter a speed of data passing through said core such that said selector is adapted to perform a speed reduction to accommodate said different operating speeds of said transmission media and said processor" as defined by independent claims 1, 8, and 15.

As shown in Applicant' Figure 2B, the multiplexers 215, 236 selectively engage a different number of data lanes 225 (e.g., alter the lane width) in order to perform a speed reduction between the transmission media 280 and the ASIC 246. For example, with the exemplary structure shown in FIG. 2B, the invention can perform speed reduction by simultaneously transmitting the data along four lanes.

To illustrate the utility of the invention, given that 12 data lanes are used in a network, when in a 4X reduction mode of operation, physical data lanes 4-11 can be used as wider extensions of lanes 0-3. Further, when in a 1X mode of operation using these 12 data lanes, FIFOs for data lanes 1-11 can be a wider extension of the FIFO used for data lane 0, thereby achieving up to a 12X speed reduction. Thus, when data is accessed at the transmission media 280, by using the multiplexers 215, 236, the upper link layer 250 can access wider data at a slower rate. The invention also produces an advantage in that receive elastic FIFO buffers 220 perform the function of the frequency correction portion 260 and correct any frequency deviations which may occur along the transmission media 280. FIFO buffers 220, 230 also modify the frequency of the signal to that desired by the ASIC 246. Therefore, the FIFO buffers 220 perform the functions that were previously performed by FIFO buffers 251 and 261 shown in FIG. 2A, thereby reducing the number of buffers within the core logic 210. This decrease in the number of buffers within the

core logic 210 reduces power consumption, increases processing speed and decreases the chip area consumed by the core logic 210.

Thus, as shown above, Aguilar does not teach or suggest selectively engaging serial data lanes to alter the data speed and Kukic also does not teach or suggest this feature. Therefore, the proposed combination of Aguilar and Kukic does not teach or suggest the claimed operation "whereby said selector selectively engages different numbers of said serial data lanes to alter a speed of data passing through said core such that said selector is adapted to perform a speed reduction to accommodate said different operating speeds of said transmission media and said processor" as defined by independent claims 1, 8, and 15. Therefore, it is Applicant's position that the proposed combination of Aguilar and Kukic does not render obvious independent claims 1, 8, and 15 and that such claims are patentable over the prior art of record. Further, dependent claims 2-6, 9-13, and 16-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

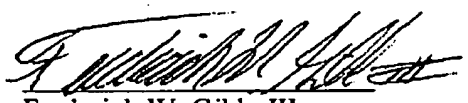
II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, Applicants submit that claims 1-6, 8-13, and 15-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



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